Implementation of Differential Chaos Shift Keying Communication System Using Matlab-Simulink

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Abstract: Spread spectrum communications have increased interest due to their immunity to channel fading and low probability of intercept. One of the limitations of the traditional digital spread spectrum systems is the need for spreading code synchronization. Chaotic communication is the analogue alternative of digital spread spectrum systems beside some extra features like simple transceiver structures. Among the chaotic modulation schemes, the Differential Chaos Shift Keying (DCSK) is the most efficient one because its demodulator detects the data without the need to chaotic signal phase recovery, i.e uses noncoherent detection. In this paper, the design of a DCSK modulator and demodulator using the efficient design tool Matlab-Simulink provided from Math work Inc. is presented. The waveforms are obtained at different stages of modulator and demodulator to allow the reader to well understand the features of this modulation type. Performance curves of DCSK are given in terms of bit-error probability versus signal to noise ratio with spreading factor as a parameter. The simulation results showed that at 10^{-3} bit error rate, 0.5 and 1 dB gains in SNR is obtained when the spreading factor is increased from 60 to 80 and 100 respectively.

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1. Introduction

Chaotic signals have the characteristic of non-periodic, random-like, inherent wideband and sensitive dependence upon initial conditions. Thus, chaotic signals have been widely applied to communication field. Broad continuous spectra of chaotic signals make them very appealing for use as carriers in spread-spectrum communications. Research in this direction has drawn considerable interest in the last few years [1-5]. At present, the studying of the chaos-based communications mainly focuses on chaotic digital communications which include chaotic digital keying modulation, chaos-based direct sequence spread spectrum, chaotic pulse position modulation, and so on. Among them, chaos keying modulation communication systems mainly include chaos shift keying (CSK)[3], chaotic on-off-keying (COOK)[4], differential chaos shift keying (DCSK)[5-7], quadrature chaos shift keying (QCSK) [8], etc. Because of sensitivity for initial conditions, it is difficult that chaotic signals realize reliably synchronization both two sides of transmitter and receiver. Therefore, non-coherent chaos communication systems which don't need chaos-synchronization are becoming a studying focus all over the world recently.

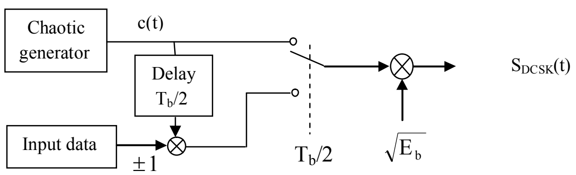
DCSK is a typical non-coherent chaos-based communication scheme, almost insensitive to channel distortion, and has good anti-noise performance. In addition, it uses the random-like characteristic of chaotic signals to reach the aim of hidden signal [7]. However, due to the length and non-periodicity of chaotic sample functions, the energy per bit is not constant and varies from one sample function to another. This problem can be solved by applying the chaotic signal to a frequency modulator [4,6]. To implement and evaluate the performance of DCSK receiver, many design tools are available. A very attractive high-level design/simulation tool is provided by MathWorksTM and is called SimulinkTM. It is a very flexible design tool, which allows testing of a high-level structural description of the design and makes possible quick changes and corrections. The circuit description structure is very similar to the way the design could be implemented later [9]. Furthermore, a lot of mapping tools, like Simulink HDL coder [10] can be used to convert Matlab-Simulink designs to hardware description codes like VDHL which can be downloaded directly to real hardware devices called Field Programmable Gate Array (FPGA) devices [11].

In this paper the design and simulation of DCSK communication systems is presented using Matlab-Simulink tool. The rest of the paper is organized as follows: section II presents a description to the DCSK communication system. Section III illustrates the design of DCSK using Matlab-Simulink tool. Section IV gives the simulation results, while section V summarizes the basic conclusions drawn throughout the work.

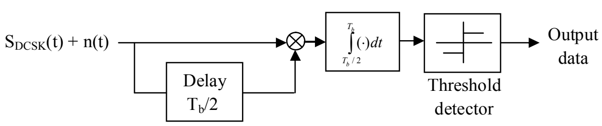
2. Differential Chaos Shift Keying Communication System

Figure 1 shows the block diagram of DCSK modulator and demodulator. In DCSK system, one bit of information is represented by two chaotic sample functions for each symbol period T_b. The first segment, c(t), is used as the reference signals, while the second, c(t-T_b/2), denotes the information-bearing signals. Information bearing signals are the replica of the reference part, and the difference between them is the sign ("+" or "-") corresponding to one bit information ("1" or "0"). The i-th symbol can be represented as:

$$S_{DCSK}(t) = \begin{cases} \sqrt{E_b}\,c(t) & 0 \le t < \frac{T_b}{2} \\ \pm\sqrt{E_b}\,c(t-\frac{T_b}{2}) & \frac{T_b}{2} \le t < T_b \end{cases} \quad (1)$$



(a)



(b)

Figure 1 Block diagram of DCSK system
(a) Modulator, (b) Demodulator

where E_b is the energy per bit. The demodulation is accomplished by a noncoherent receiver which is, in fact, a bit-energy estimator. In the receiver the ith digital information is extracted by computing the correlation between two received sample functions:

$$\int_{(i-1)T_b}^{iT_b} S_{DCSK}(t)\, S_{DCSK}(t-T_b/2)\,dt \quad (2)$$

Then, the output of the correlator is sampled over each symbol period and the decision threshold is usually determined to be zero. If the output is positive then the extracted data is declared to be "1", otherwise it is declared to be "0".

3. Matlab-Simulink Implementation

Figure 2 shows the Matlab-Simulink implementation of DCSK system. The detailed block of the chaotic generator is shown in Figure 3. The chaotic generator is based on Hennon map given by:

$$x_{n+1} = 1 + bx_n + ax_n^2 \quad (3)$$

where a and b are constants and a=-1.4 and b=0. Assuming each data bit contains 100 chaotic sample, the spreading factor is defined as β (i.e β = 100). Therefore, to achieve half data duration delay (i.e T_b/2), a delay block with 50 samples (z^{-50} block) is used. A random data is generated using unipolar Bernoulli source which is then converted to bipolar format to achieve the multiplication operations with the chaotic signal correctly. Two pulse generators are used with 50% duty cycle are used together with multipliers and summer to generate equation 1. *Pulse generator* block produces ON pulse in the first half of bit duration to send the reference chaotic signal and becomes OFF in the second half. *Pulse generator 1* operates in opposite way, i.e. it stays OFF in the first half of bit duration and becomes ON in the second half to allow the delayed chaotic signal. In the second half of data bit duration, the chaotic signal is either stay as it is, i.e. c(t-T_b/2) or inverted, i.e. –c(t-T_b/2), depending on the value of data using the unipolar to bipolar converter. The channel is assumed to be AWGN which is available at communication blockset in Matlab-Simulink library.

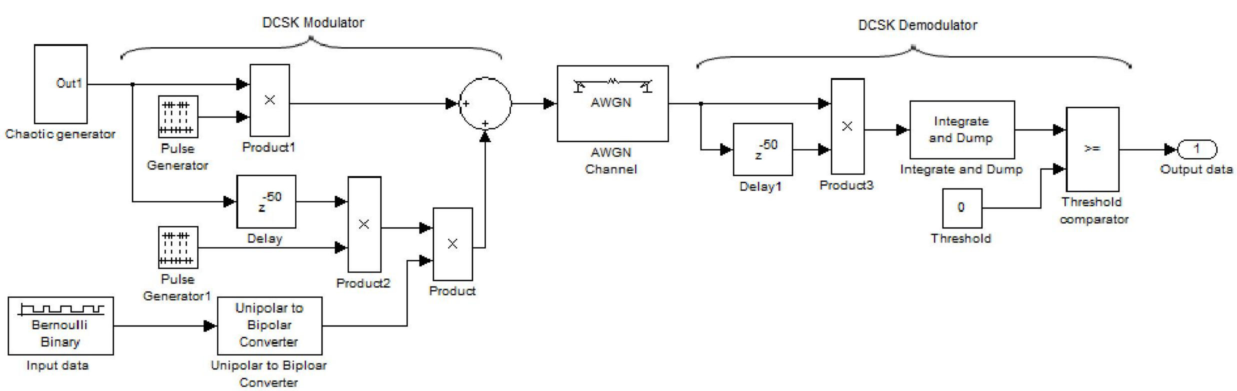


Figure 2 Matlab-Simulink implementation of DCSK system

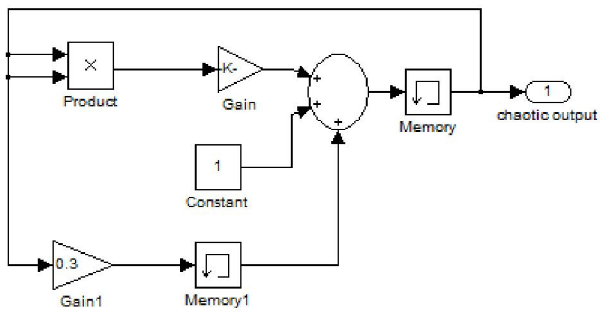


Figure 3 Matlab-Simulink implementation of Hennon chaotic map.

The demodulator is differentially coherent with the modulator where the received chaotic signal is correlated with a delayed replica of itself to produce a decision variable. Therefore the *delay* block is used once again in the Simulink design of the demodulator as shown in Figure 1. The *integrate and dump* block is used to perform the correlation while the *threshold comparator* block decides whether the output data is "1" or "0" after comparing the value resulted from the correlator with the threshold value which is set to zero.

4. Simulation Results

The Matlab-Simulink results obtained are divided into two parts: the waveforms obtained from the simulation and the bit error rate performance curves. Figure 4 shows the generated chaotic signal with its auto correlation values. The time scale of this figure is enlarged to show the random nature of the chaotic signal. The values of the chaotic signal is bounded by -1 and +1 values which agrees with the expected outcome from Hennon map given in equation 1. In the same figure to the down, the autocorrelation function of the generated chaotic signal is displayed. It can be seen from the autocorrelation values that the chaotic signal is really a random signal like nosie where the signal does not matches itself only when the phase shift is zero, i.e autocorrelation is 1 only at t=0. However, ideally the autocorrelation value at time epochs other than zero should be zero, but in our case some higher values are exist due to limited number of points considered.

Figure 5 shows the simulation waveforms of the implemented transmitter. Fig.5a shows the data to be transmitted while Fig.5b shows the generated chaotic signal. In this figure the duration of each data signal contains 100 chaotic samples, i.e. β=100. In our simulations, three values for β are considered those are: 100, 80 and 60. Fig.5c shows the transmitted DCSK signal. It can be seen in this figure that the transmitted is looks like noise and the points where the phase of chaotic carrier is changed cannot be recognized by human eyes due the high spreading factor and the noisy like nature of the chaotic signal.

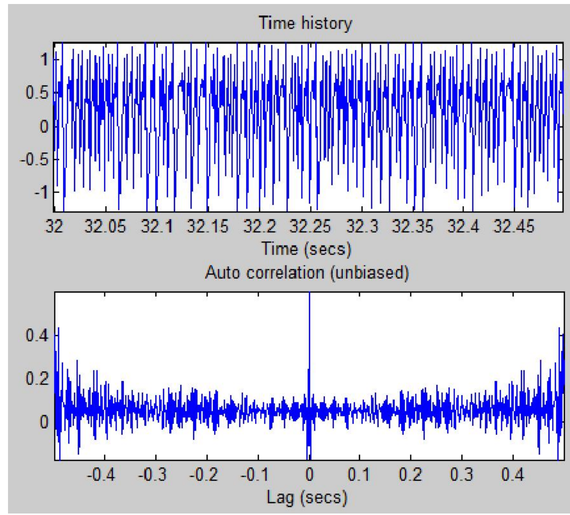


Figure 4 Chaotic signal generator output with the corresponding autocorrelation.

Figure 6 shows the demodulator simulation waveforms. Figure 6a depicts the received DCSK signal plus noise. In this figure the signal to noise ratio was 15 dB. Since the effect of noise is not so strong, the waveform looks like that in Figure 5c. Figure 6b shows the received signal multiplied by a shifted version of itself by $T_b/2$ (or 50 chaotic samples if β=100). It is clear from this figure that the boundaries of data are started to occur. The chaotic samples are grouped to be either positive or negative along half bit duration. However, there is a little amount of positive samples within a majority of negative ones and vice versa due to additive noise. Figure 6c shows the integrator output at the demodulator. The integrator accumulates the chaotic samples after the multiplier along half bit duration. We get positive integrator results when the data bit is "1" and negative results when the data bit is "0".

Therefore, setting the threshold to zero will extract successfully the data as shown in Figure 6d. It is worth noted the decision is made every bit duration to get right data intervals.

Finally, Figure 7 shows the performance curves of the designed DCSK system in AWGN superior performance where it lags only 2dB behind BPSK, standard digital modulation scheme. Also it can be noticed from the figure that as the spreading factor is increased the channel with spreading factor as a parameter. It can be seen in this figure that the bit error probability is reduced significantly when the signal-to-noise ratio (SNR) is increased and 10^{-3} bit error rate is obtained when the signal-to-noise ratio is about 9 dB. It is considered as performance of DCSK is improved. At

10^{-3} bit error rate, 0.5 and 1 dB gains in SNR are obtained when the spreading factor is increased from 60 to 80 and 100 respectively.

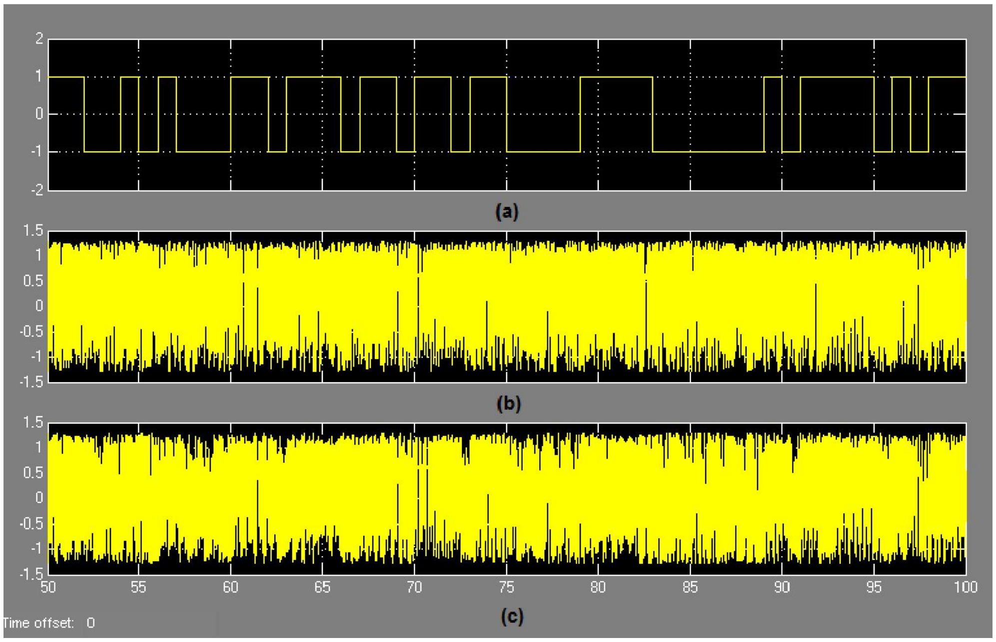


Figure 5 Simulation waveforms of the DCSK transmitter
(a) Transmitted data, (b) Chaotic carrier with β=100, (c) DCSK waveform

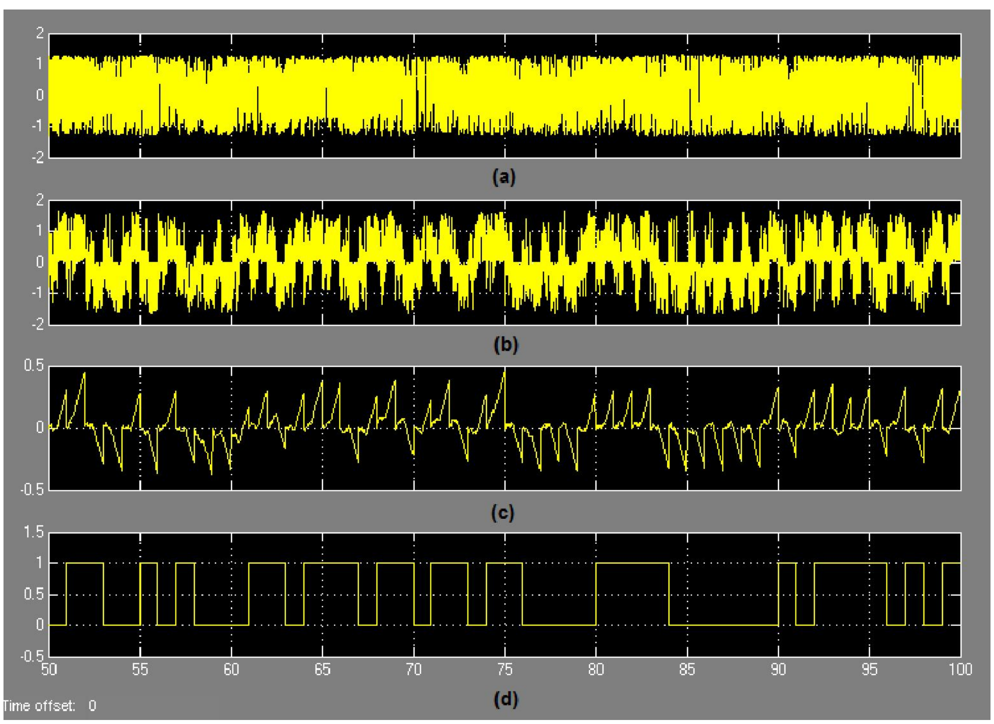


Figure 6 Simulation waveforms of the DCSK receiver
(a) Received signal with noise r(t), (b) Waveform of $r(t).r(t-T_b/2)$
(c) Integrator output, (d) The detected data

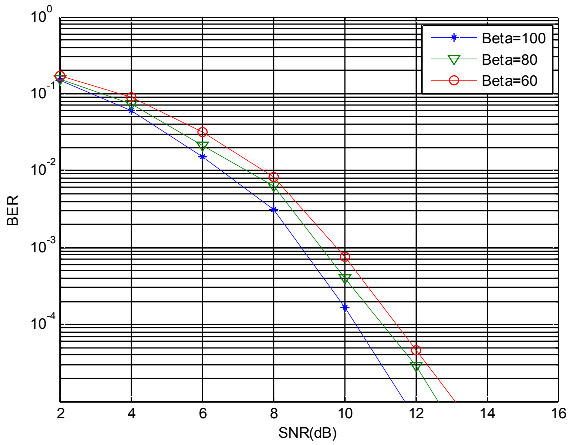


Figure 7. Performance of the simulated DCSK at different values of the spreading factor.

5. Conclusions

The differential chaos shift keying is most efficient chaotic modulation scheme due to its simplicity, noncoherent detection capability and good bit error rate performance in noisy channel. To achieve better bit error rate performance, the spreading factor which represents the number of chaotic samples per data bit duration should be as max as possible. The implementation of DCSK system can be done using different approaches. However, the use of Matlab-Simulink design tool to perform the design have many positive features like fast and flexible design cycle due its structural nature, easy changing the simulation parameter and the compatibility with conversion tools that can access real hardware devices.

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